



# 12-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

MAX5742

## General Description

The MAX5742 quad, 12-bit, low-power, buffered voltage-output, digital-to-analog converter (DAC) is packaged in a space-saving 10-pin  $\mu$ MAX package (5mm x 3mm). The wide supply voltage range of +2.7V to +5.5V and 229 $\mu$ A supply current accommodates low-power and low-voltage applications. DAC outputs employ on-chip precision output amplifiers that swing Rail-to-Rail<sup>®</sup>. The MAX5742's reference input accepts a voltage range from 0 to  $V_{DD}$ . In power-down the reference input is high impedance, further reducing the system's total power consumption.

The 20MHz, 3-wire SPI<sup>™</sup>, QSPI<sup>™</sup>, MICROWIRE<sup>™</sup> and DSP-compatible serial interface saves board space and reduces the complexity of opto- and transformer-isolated applications. The MAX5742 on-chip power-on reset (POR) circuit resets the DAC outputs to zero and loads the output with a 100k $\Omega$  resistor to ground. This provides additional safety for applications that drive valves or other transducers that need to be off on power-up. The MAX5742's software-controlled power-down reduces supply current to less than 0.3 $\mu$ A and provides software-selectable output loads (1k $\Omega$ , 100k $\Omega$ , or high impedance) while in power-down. The MAX5742 is specified over the -40 $^{\circ}$ C to +125 $^{\circ}$ C automotive temperature range.

## Applications

Automatic Tuning  
Gain and Offset Adjustment  
Power Amplifier Control  
Process Control I/O Boards  
Battery-Powered Instruments  
VCO Control

**Functional Diagram appears at end of data sheet.**

*Rail-to-Rail is a registered trademark of Nippon Motorola, Inc.  
SPI and QSPI are trademarks of Motorola, Inc.  
MICROWIRE is a trademark of National Semiconductor, Corp.*

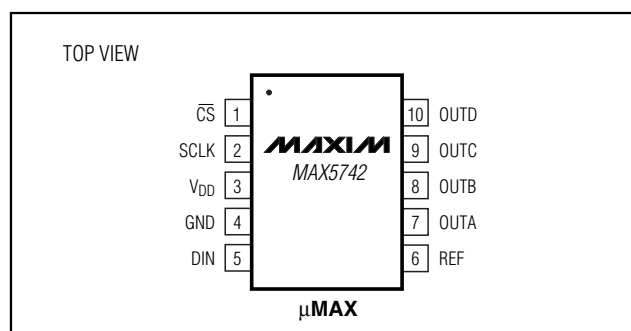
## Features

- ◆ Ultra-Low Power Consumption  
229 $\mu$ A at  $V_{DD} = +3.6V$   
271 $\mu$ A at  $V_{DD} = +5.5V$
- ◆ Wide +2.7V to +5.5V Single-Supply Range
- ◆ 10-Pin  $\mu$ MAX Package
- ◆ 0.3 $\mu$ A Power-Down Current
- ◆ Guaranteed 12-Bit Monotonicity ( $\pm 1$ LSB DNL)
- ◆ Safe Power-Up Reset to Zero Volts at DAC Output
- ◆ Three Software-Selectable Power-Down Impedances (100k $\Omega$ , 1k $\Omega$ , Hi-Z)
- ◆ Fast 20MHz 3-Wire SPI, QSPI, and MICROWIRE-Compatible Serial Interface
- ◆ Rail-to-Rail Output Buffer Amplifiers
- ◆ Schmitt-Triggered Logic Inputs for Direct Interfacing to Optocouplers
- ◆ Wide -40 $^{\circ}$ C to +125 $^{\circ}$ C Operating Temperature Range

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5742EUB	-40 $^{\circ}$ C to +85 $^{\circ}$ C	10 $\mu$ MAX
MAX5742AUB	-40 $^{\circ}$ C to +125 $^{\circ}$ C	10 $\mu$ MAX

## Pin Configuration



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## ABSOLUTE MAXIMUM RATINGS

V<sub>DD</sub> to GND .....-0.3V to +6V  
 OUT<sub>-</sub>, SCLK, DIN,  $\overline{\text{CS}}$ , REF to GND .....-0.3 to (V<sub>DD</sub>+0.3V)  
 Maximum Continuous Current Into Any Pin .....±50mA  
 Continuous Power Dissipation (T<sub>A</sub> = +70°C)  
 10-Pin  $\mu$ MAX (derate 6.9 mW/°C above +70°C) .....555mW

Operating Temperature Range .....-40°C to +125°C  
 Junction Temperature .....-65°C to +150°C  
 Storage Temperature Range .....-65°C to +150°C  
 Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +2.7V to +5.5V, GND = 0, V<sub>REF</sub> = V<sub>DD</sub>, R<sub>L</sub> = 5k $\Omega$ , C<sub>L</sub> = 200pF, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are V<sub>DD</sub> = +5V, T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>STATIC ACCURACY</b> (Note 1)						
Resolution	N		12			Bits
Integral Nonlinearity Error	INL	(Note 2)		±2	±16	LSB
Differential Nonlinearity Error	DNL	Guaranteed monotonic (Note 2)			±1	LSB
Zero-Code Error	OE	Code = 000		0.4	1.5	% of FS
Zero-Code Error Tempco				2.3		ppm/°C
Gain Error	GE	Code = FFF hex			±3	% of FS
Gain-Error Tempco				0.26		ppm/°C
Power-Supply Rejection Ratio	PSRR	Code = FFF hex, $\Delta$ V <sub>DD</sub> = ±10%		58.8		dB
<b>REFERENCE INPUT</b>						
Reference Input Voltage Range	V <sub>REF</sub>		0		V <sub>DD</sub>	V
Reference Input Impedance	R <sub>REF</sub>	In operation	32	45	63	k $\Omega$
		In power-down mode		2		M $\Omega$
Power-Down Reference Current		In power-down mode (Note 3)		1	10	$\mu$ A
<b>DAC OUTPUT</b>						
Output Voltage Range		No load (Note 4)	0		V <sub>DD</sub>	V
DC Output Impedance		Code = 800 hex		0.8		$\Omega$
Short-Circuit Current		V <sub>DD</sub> = +3V		15		mA
		V <sub>DD</sub> = +5V		48		
Wake-Up Time		V <sub>DD</sub> = +3V		8		$\mu$ s
		V <sub>DD</sub> = +5V		8		
Output Leakage Current		Power-down mode = output high impedance		±18		nA

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +2.7V$  to  $+5.5V$ ,  $GND = 0$ ,  $V_{REF} = V_{DD}$ ,  $R_L = 5k\Omega$ ,  $C_L = 200pF$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are  $V_{DD} = +5V$ ,  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DIGITAL INPUTS (SCLK, DIN, <math>\overline{CS}</math>)</b>						
Input High Voltage	$V_{IH}$	$V_{DD} = +3V, +5V$	0.7 x $V_{DD}$			V
Input Low Voltage	$V_{IL}$	$V_{DD} = +3V, +5V$			0.3 x $V_{DD}$	V
Input Leakage Current	$I_{IN}$	Digital inputs = 0 or $V_{DD}$		$\pm 0.1$	$\pm 1$	$\mu A$
Input Capacitance	$C_{IN}$			5		pF
<b>DYNAMIC PERFORMANCE</b>						
Voltage Output Slew Rate	SR			0.5		V/ $\mu s$
Voltage Output Settling Time		400 hex to C00 hex (Note 5)		4	10	$\mu s$
Digital Feedthrough		Any digital inputs from 0 to $V_{DD}$		0.1		nV-s
Digital-Analog Glitch Impulse		Major carry transition (code 7FF hex to code 800 hex)		12		nV-s
DAC-to-DAC Crosstalk				2.4		nV-s
<b>POWER REQUIREMENTS</b>						
Supply-Voltage Range	$V_{DD}$		2.7		5.5	V
Supply Current with No Load	$I_{DD}$	All digital inputs at 0 or $V_{DD} = 3.6V$		229	395	$\mu A$
		All digital inputs at 0 or $V_{DD} = 5.5V$		271	420	
Power-Down Supply Current	$I_{DDPD}$	All digital inputs at 0 or $V_{DD} = 5.5V$		0.29	1	$\mu A$

## TIMING CHARACTERISTICS

( $V_{DD} = 2.7V$  to  $5.5V$ ,  $GND = 0$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Frequency	$f_{SCLK}$		0		20	MHz
SCLK Pulse Width High	$t_{CH}$		25			ns
SCLK Pulse Width Low	$t_{CL}$		25			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	$t_{CSS}$		10			ns
SCLK Fall to $\overline{CS}$ Rise Setup Time	$t_{CSH}$		10			ns
DIN to SCLK Fall Setup Time	$t_{DS}$		15			ns
DIN to SCLK Fall Hold Time	$t_{DH}$		0			ns
$\overline{CS}$ Pulse Width High	$t_{CSW}$		80			ns

**Note 1:** DC specifications are tested without output loads.

**Note 2:** Linearity guaranteed from code 115 to code 3981.

**Note 3:** Limited with test conditions.

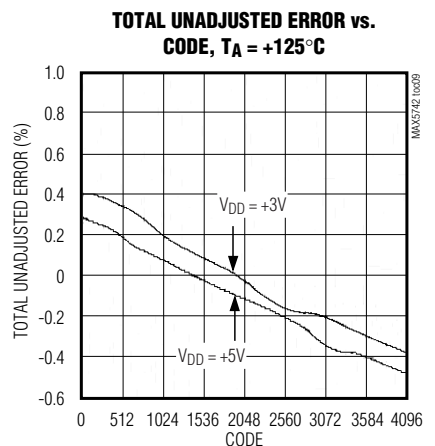
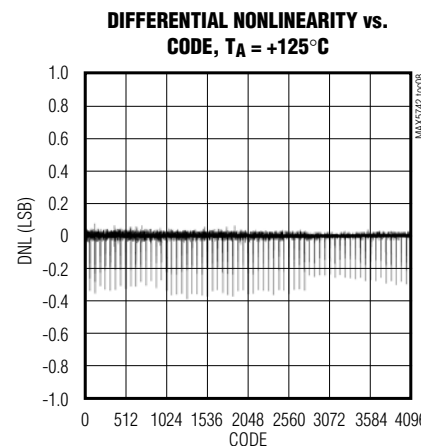
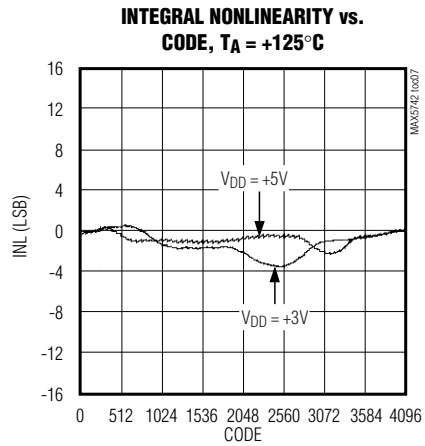
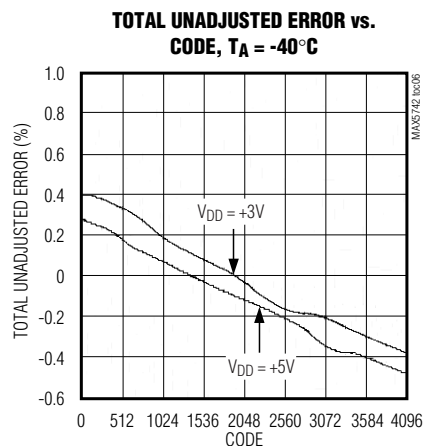
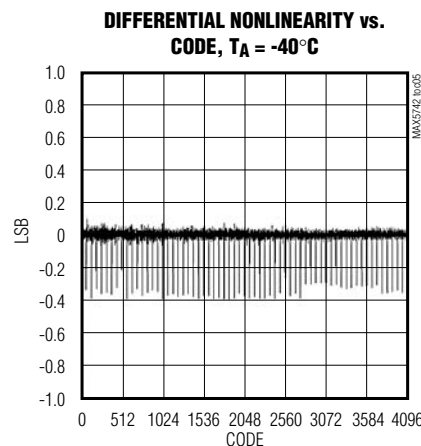
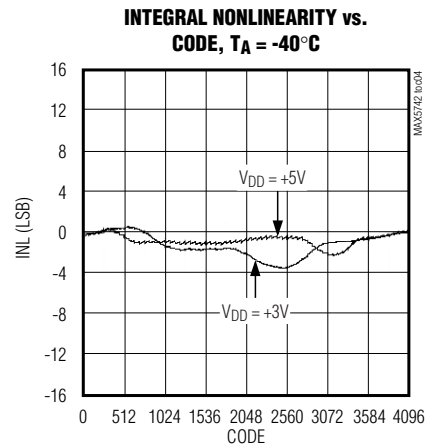
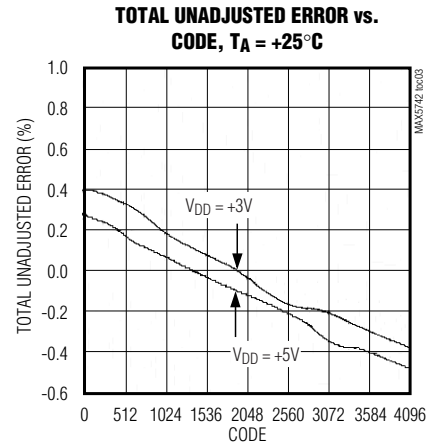
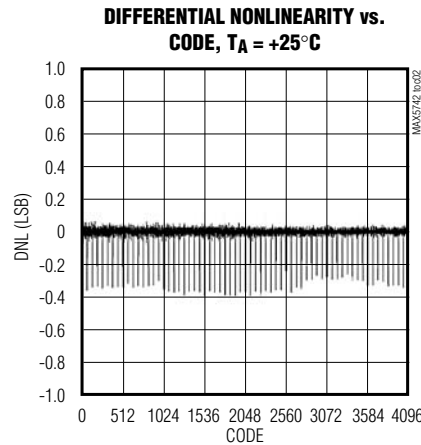
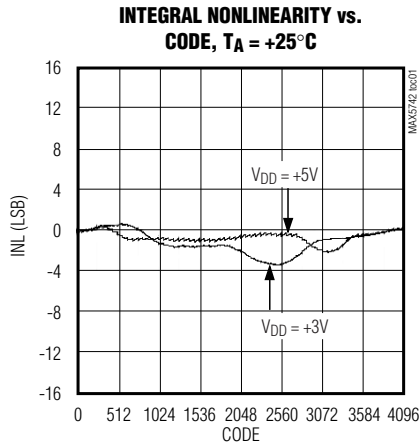
**Note 4:** Offset and gain error limit the FSR.

**Note 5:** Guaranteed by design.

# 12-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

## Typical Operating Characteristics

( $V_{REF} = V_{DD}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



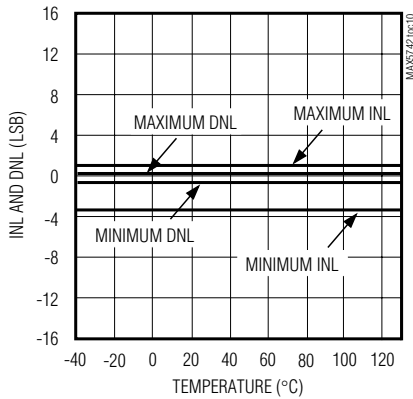
# 12-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

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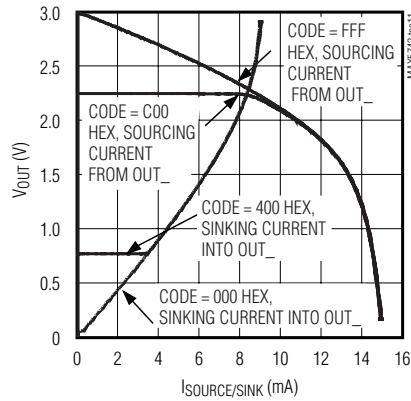
## Typical Operating Characteristics (continued)

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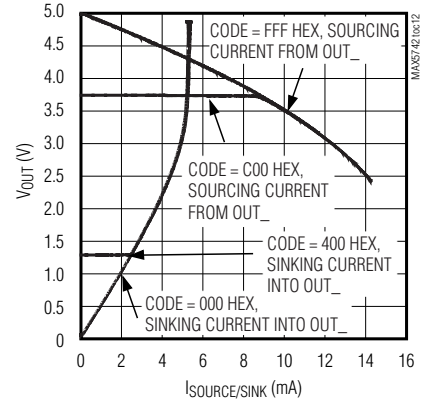
**WORST-CASE INL AND DNL vs. TEMPERATURE**



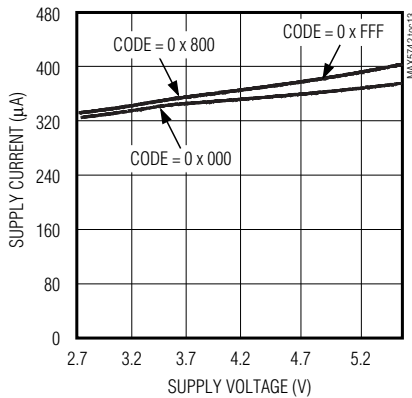
**SOURCE-AND-SINK CURRENT CAPABILITY ( $V_{DD} = +3V$ )**



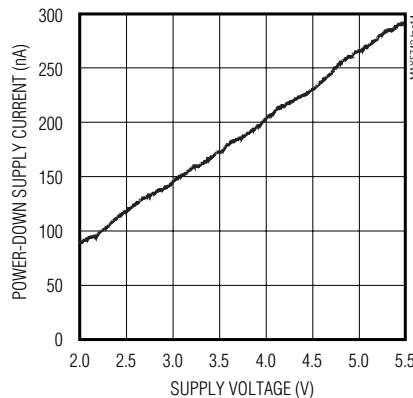
**SOURCE-AND-SINK CURRENT CAPABILITY ( $V_{DD} = +5V$ )**



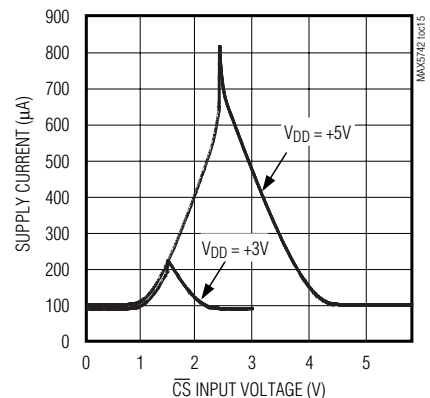
**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



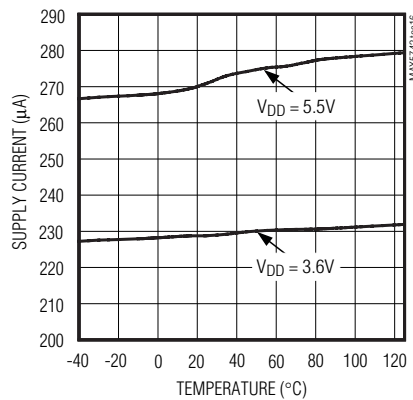
**POWER-DOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE**



**SUPPLY CURRENT vs.  $\overline{CS}$  INPUT VOLTAGE**



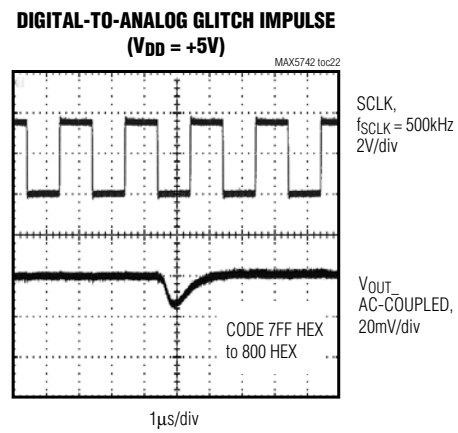
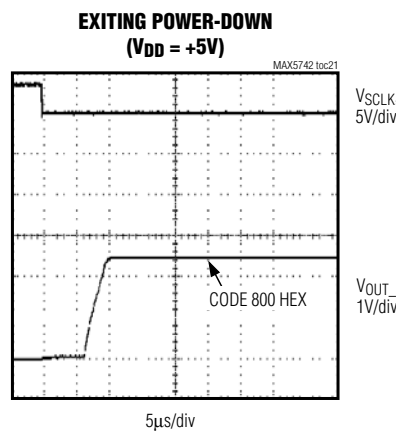
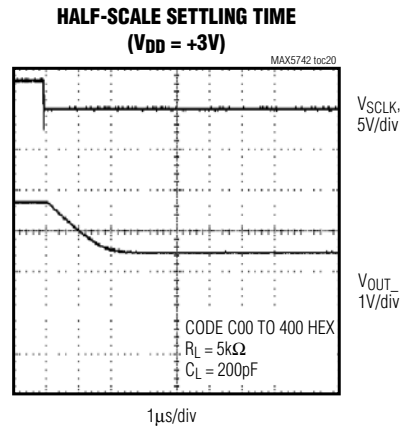
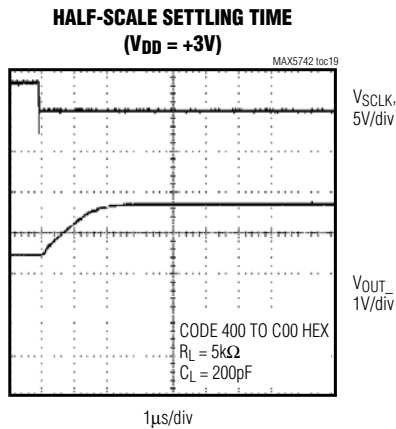
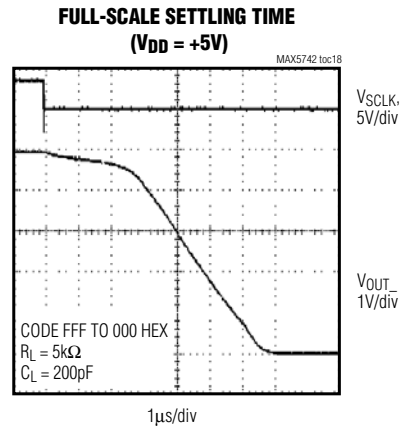
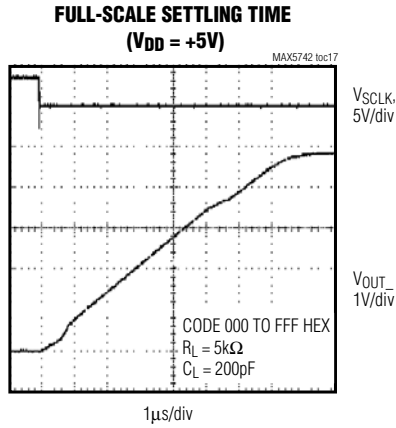
**SUPPLY CURRENT vs. TEMPERATURE**



# 12-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

## Typical Operating Characteristics (continued)

( $V_{REF} = V_{DD}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



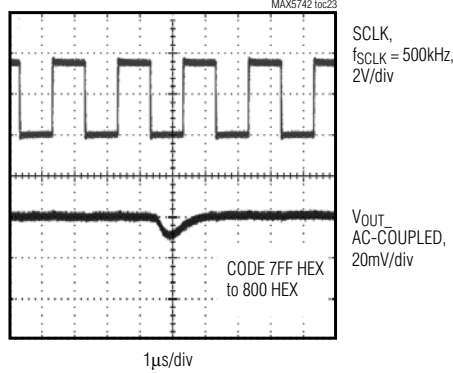
# 12-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

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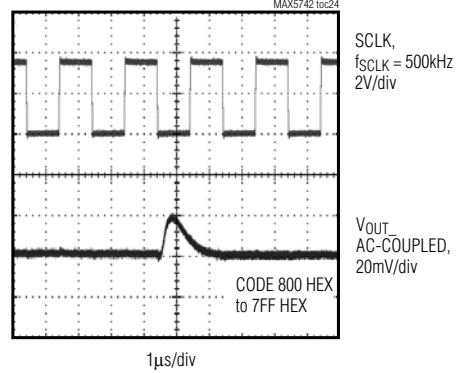
## Typical Operating Characteristics (continued)

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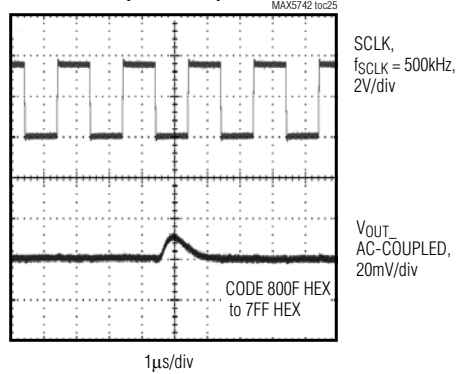
**DIGITAL-TO-ANALOG GLITCH IMPULSE**  
( $V_{DD} = +3V$ )



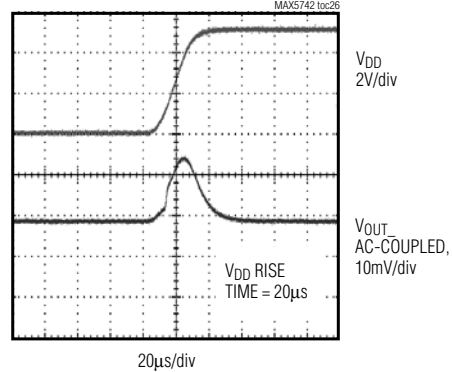
**DIGITAL-TO-ANALOG GLITCH IMPULSE**  
( $V_{DD} = +5V$ )



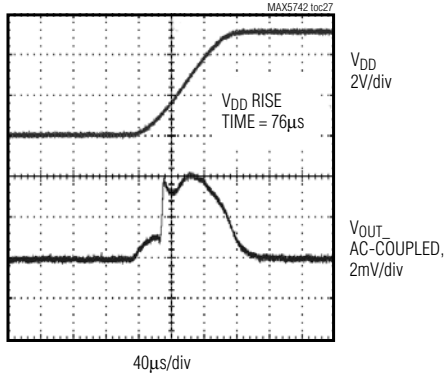
**DIGITAL-TO-ANALOG GLITCH IMPULSE**  
( $V_{DD} = +3V$ )



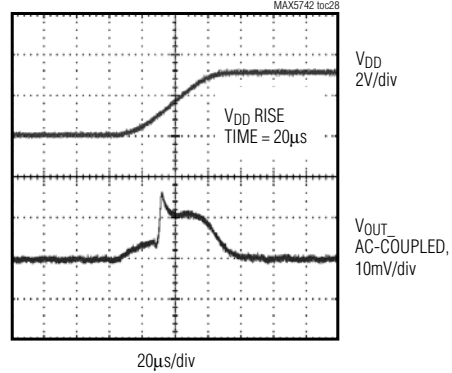
**POWER-ON RESET, FAST RISE TIME**  
( $V_{DD} = +5V$ )



**POWER-ON RESET, SLOW RISE TIME**  
( $V_{DD} = +5V$ )



**POWER-ON RESET, FAST RISE TIME**  
( $V_{DD} = +3V$ )

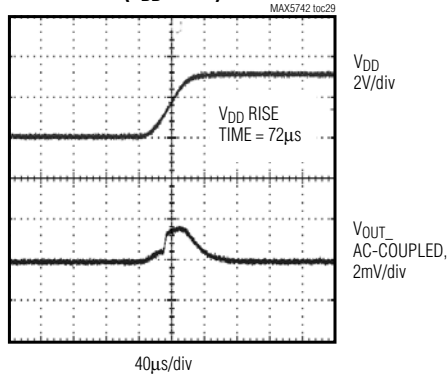


# 12-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

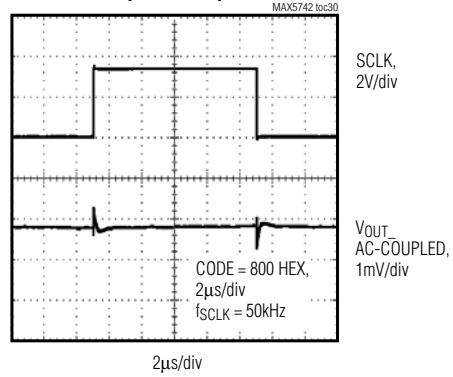
## Typical Operating Characteristics (continued)

( $V_{REF} = V_{DD}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

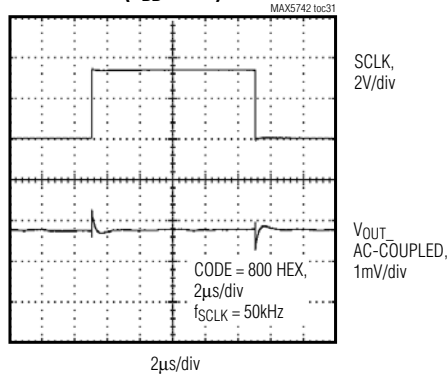
**POWER-ON RESET, SLOW RISE-TIME**  
( $V_{DD} = +3\text{V}$ )



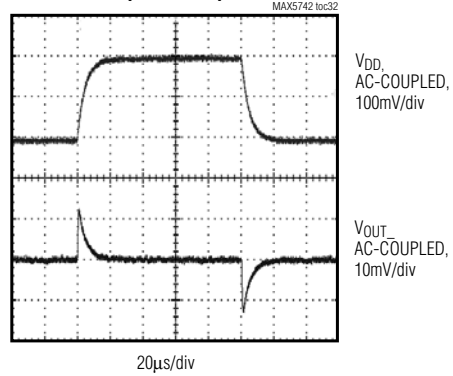
**CLOCK FEEDTHROUGH**  
( $V_{DD} = +5\text{V}$ )



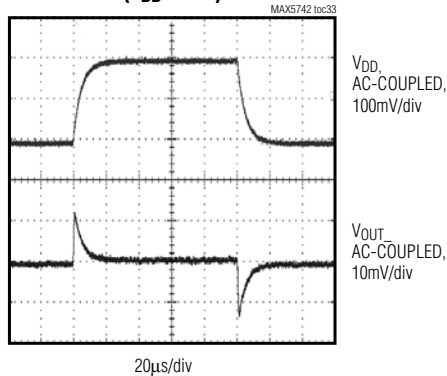
**CLOCK FEEDTHROUGH**  
( $V_{DD} = +3\text{V}$ )



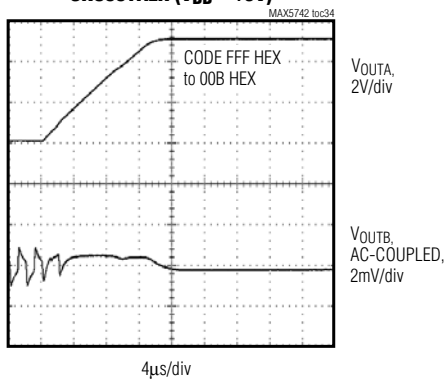
**LINE TRANSIENT RESPONSE**  
( $V_{DD} = +5\text{V}$ )



**LINE TRANSIENT RESPONSE**  
( $V_{DD} = +3\text{V}$ )



**CROSSTALK ( $V_{DD} = +5\text{V}$ )**





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## Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{CS}}$	Chip-Select Input
2	SCLK	Serial-Clock Input
3	V <sub>DD</sub>	Power-Supply Input
4	GND	Ground
5	DIN	Serial Data Input
6	REF	External Reference Voltage Input
7–10	OUTA –OUTD	DAC Voltage Outputs. Power-on reset sets DAC registers to zero, and internally connects OUT to GND with 100kΩ resistor.

## Detailed Description

The MAX5742 contains four 12-bit, voltage-output, low-power digital-to-analog converters (DACs). Each DAC employs a resistor string architecture that converts a 12-bit digital input word to an equivalent analog output voltage proportional to the applied reference voltage. The MAX5742 shares one reference input (REF) between all four DACs. The MAX5742 includes rail-to-rail output buffer amplifiers for each DAC, and input logic for simple microprocessor (μP), and CMOS interfaces. The power-supply range is from +2.7V to +5.5V (*Functional Diagram*). The MAX5742's reference input accepts a voltage range from 0 to V<sub>DD</sub>. In power-down mode the reference input is high impedance. The MAX5742 is compatible with the 3-wire SPI, QSPI, MICROWIRE and DSP serial interface with Schmitt-triggered logic inputs.

### Reference Input and DAC Output Range

The reference input accepts positive DC and AC signals. The voltage at REF sets the full-scale output voltage of the four DACs. The reference input voltage range is 0 to V<sub>DD</sub>. The impedance at REF is 45kΩ. The voltage at REF can vary from GND to V<sub>DD</sub>. The output voltages (V<sub>OUT\_</sub>) are represented by a digitally programmable voltage source as:

$$V_{OUT\_} = (V_{REF} \times D) / 2^{12}$$

where D is the decimal equivalent of binary DAC input code ranging from 0 to 4095. V<sub>REF</sub> is the voltage at REF.

### Output Buffer Amplifiers

All DACs are internally buffered at the output. The buffer amplifiers have both rail-to-rail common mode

and (GND to V<sub>REF</sub>) output voltage range. The buffers are unity-gain stable with C<sub>L</sub> = 200pF and R<sub>L</sub> = 5kΩ. Buffer amplifiers are disabled during power-up and individual DAC outputs are shorted to GND through a 100kΩ resistor. Buffer amplifiers can individually or altogether be powered-down by programming the input register control bits. During power down, contents of the input and DAC registers remain the same. On wake-up, all DAC outputs are restored to their pre-power-down voltage values.

### Power-Down Mode

In power-down mode, the DAC outputs are programmed to one of three output states, 1kΩ, 100kΩ, or floating (Table 1). The REF input is high impedance (2MΩ typ) to conserve current drain from the system reference; therefore, the system reference does not have to be powered-down. The DAC outputs return to the values contained in the registers when brought out of power-down. The recovery time, from total power-down to power-up, is 8μs. This extra time is needed to allow the internal bias to wake-up. Power-down mode reduces current consumption to 0.3μA.

### 3-Wire Serial Interface

The MAX5742 digital interface is a standard 3-wire connection compatible with SPI/QSPI/MICROWIRE/DSP interfaces. The chip-select input ( $\overline{\text{CS}}$ ) frames the serial data loading at DIN. Immediately following  $\overline{\text{CS}}$  high-to-low transition, the data is shifted synchronously and latched into the input register on the falling edge of the serial clock input (SCLK). After 16 bits have been loaded into the serial input register, it transfers its contents to the DAC latch.  $\overline{\text{CS}}$  may then either be held low or brought high.  $\overline{\text{CS}}$  must be brought high for a minimum of 80ns before the next write sequence, since a

# 12-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

Table 1. Power-Down Mode Control

EXTENDED CONTROL				DATA BITS						DESCRIPTION	FUNCTION
C3	C2	C1	C0	D11–D5	D4	D3	D2	D1	D0		
1	1	1	1	X	0	0	0	0	0	DAC A	DAC O/P, wakeup
1	1	1	1	X	0	0	0	0	1	DAC A	Floating output
1	1	1	1	X	0	0	0	1	0	DAC A	Output is terminated with 1kΩ
1	1	1	1	X	0	0	0	1	1	DAC A	Output is terminated with 100kΩ
1	1	1	1	X	0	0	1	0	0	DAC B	DAC O/P, wakeup
1	1	1	1	X	0	0	1	0	1	DAC B	Floating output
1	1	1	1	X	0	0	1	1	0	DAC B	Output is terminated with 1kΩ
1	1	1	1	X	0	0	1	1	1	DAC B	Output is terminated with 100kΩ
1	1	1	1	X	0	1	0	0	0	DAC C	DAC O/P, wakeup
1	1	1	1	X	0	1	0	0	1	DAC C	Floating output
1	1	1	1	X	0	1	0	1	0	DAC C	Output is terminated with 1kΩ
1	1	1	1	X	0	1	0	1	1	DAC C	Output is terminated with 100kΩ
1	1	1	1	X	0	1	1	0	0	DAC D	DAC O/P, wakeup
1	1	1	1	X	0	1	1	0	1	DAC D	Floating output
1	1	1	1	X	0	1	1	1	0	DAC D	Output is terminated with 1kΩ
1	1	1	1	X	0	1	1	1	1	DAC D	Output is terminated with 100kΩ
1	1	1	1	X	1	0	0	0	0	DAC A-D	DAC O/P, wakeup
1	1	1	1	X	1	0	0	0	1	DAC A-D	Floating output
1	1	1	1	X	1	0	0	1	0	DAC A-D	Output is terminated with 1kΩ
1	1	1	1	X	1	0	0	1	1	DAC A-D	Output is terminated with 100kΩ

X = Don't care

write sequence is initiated on a falling edge of  $\overline{CS}$ . Not keeping  $\overline{CS}$  low during the first 15 SCLK cycles discards input data. The serial clock (SCLK) can idle either high or low between transitions. Table 2 lists serial-interface programming commands.

### Power-On Reset (POR)

The MAX5742 has an internal POR circuit. At power-up all DACs are powered-down and  $OUT_{-}$  is terminated to GND through 100kΩ resistors. Contents of input and DAC registers are cleared to all zero. An 8μs recovery time after issuing a wake-up command is needed before writing to the DAC registers. Power-down mode control commands can be applied immediately with no recovery time.

C3-C0 are control bits. The data bits D11 to D0 are in straight binary format. All zeros correspond to zero scale and all ones correspond to full scale.

### Digital Inputs

The digital inputs are compatible with CMOS logic. In order to save power and reduce input to output coupling, SCLK and DIN input buffers are powered down immediately after completion of shifting 16 bits into the input shift register. A high to low transition at  $\overline{CS}$  powers up SCLK and DIN input buffers.

# 12-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

CONTENTS OF SHIFT REGISTER															
D15 (MSB)														D0 (LSB)	
C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 1. 16-Bit Input Word

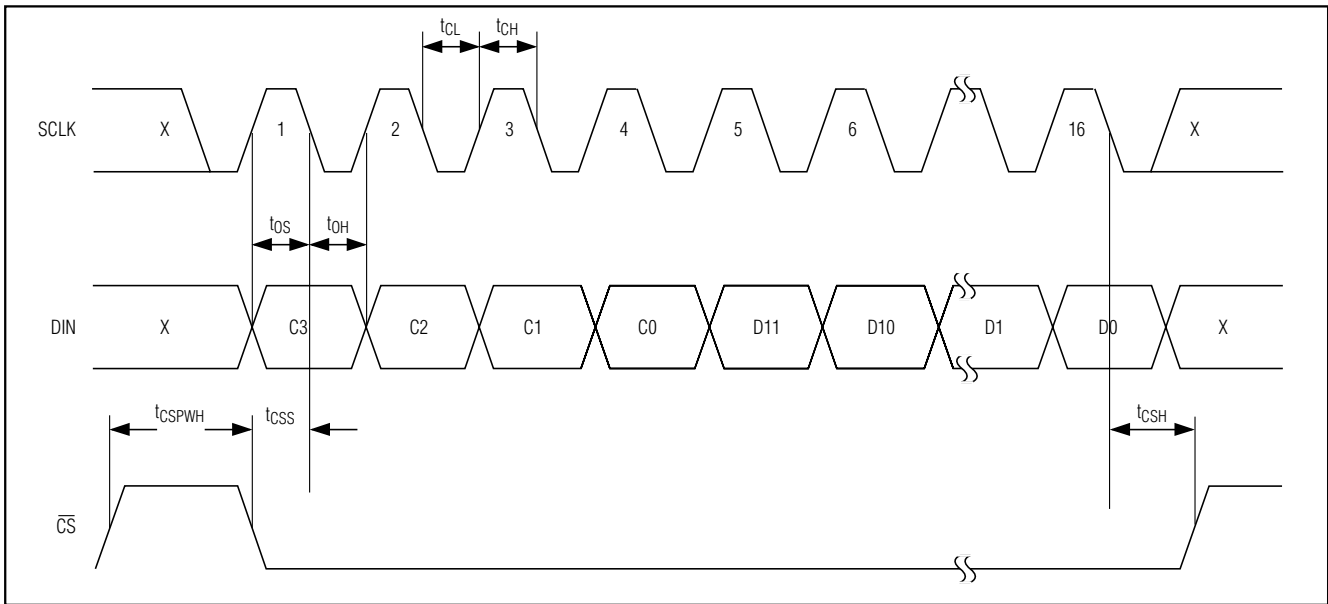


Figure 2. Timing Diagram

## Applications Information

### Unipolar Output

The typical application circuit (Figure 3) shows the MAX5742 configured for a unipolar output, where the output voltages and the reference inputs have the same polarity. Table 3 lists the unipolar output codes.

### Bipolar Output

The MAX5742 can be configured for bipolar operation using a dual supply op amp (Figure 4). The transfer function for bipolar operation is:

$$V_{OUT} = V_{REF} \left[ \left( \frac{2NB}{4096} \right) - 1 \right]$$

where NB is the decimal value of the DAC's binary input code. Table 4 shows digital codes (offset binary) and corresponding output voltages for the circuit in Figure 4.

### Power Supply and Layout Considerations

Careful PC board layout is important for optimal system performance. To reduce noise injection and digital feed-through, keep analog and digital signals separate. Ensure that the return path from GND to the supply ground is short and low impedance. Use a ground plane. Bypass  $V_{DD}$  to GND with a 0.1 $\mu$ F capacitor as close as possible to  $V_{DD}$ .

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**Table 2. Serial-Interface Programming Commands**

CONTROL				DATA BITS	DAC	FUNCTION
C3	C2	C1	C0	D11-D00		
0	0	0	0	X	A	Shift reg through DAC reg, O/P updated
0	0	0	1	X	B	Shift reg through DAC reg, O/P updated
0	0	1	0	X	C	Shift reg through DAC reg, O/P updated
0	0	1	1	X	D	Shift reg through DAC reg, O/P updated
0	1	0	0	X	A	Shift reg through I/P reg, O/P unchanged
0	1	0	1	X	B	Shift reg through I/P reg, O/P unchanged
0	1	1	0	X	C	Shift reg through I/P reg, O/P unchanged
0	1	1	1	X	D	Shift reg through I/P reg, O/P unchanged
1	0	0	0	X	A	I/P reg through DAC reg, O/P updated
1	0	0	1	X	B	I/P reg through DAC reg, O/P updated
1	0	1	0	X	C	I/P reg through DAC reg, O/P updated
1	0	1	1	X	D	I/P reg through DAC reg, O/P updated
1	1	0	0	X	A-D	Shift reg through DAC reg, O/P updated
1	1	0	1	X	A-D	Shift reg through I/P reg, O/P unchanged
1	1	1	0	X	A-D	I/P reg through DAC reg, O/P updated

X = Don't care

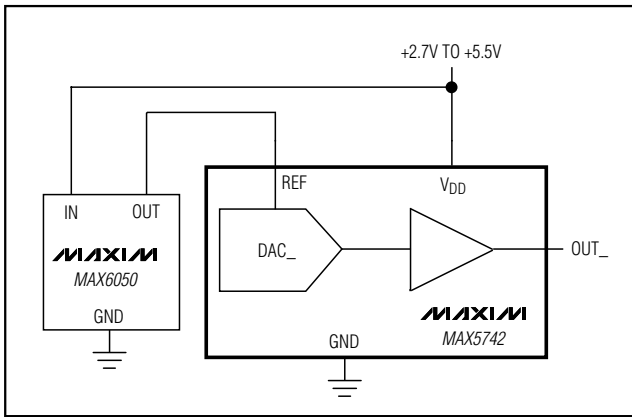


Figure 3. Typical Operating Circuit, Unipolar Output

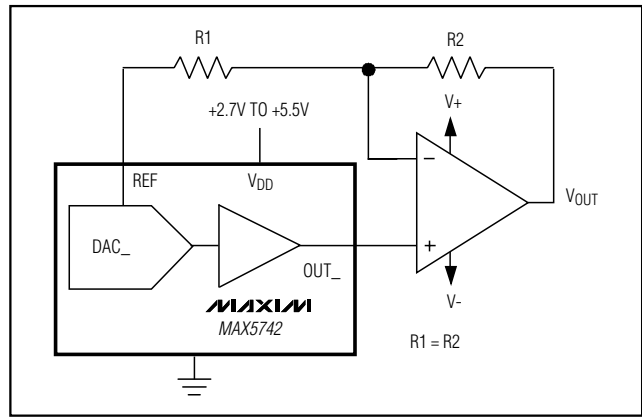


Figure 4. Bipolar Output Circuit

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MAX5742

**Table 3. Unipolar Code Table**

DAC CONTENTS	ANALOG OUTPUT
1111 1111 1111	$V_{REF} \left( \frac{4095}{4096} \right)$
1000 0000 0001	$V_{REF} \left( \frac{2049}{4096} \right)$
1000 0000 0000	$\frac{V_{REF}}{2}$
0111 1111 1111	$V_{REF} \left( \frac{2047}{4096} \right)$
0000 0000 0001	$V_{REF} \left( \frac{1}{4096} \right)$
0000 0000 0000	0

**Table 4. Bipolar Code Table**

DAC CONTENTS	ANALOG OUTPUT
1111 1111 1111	$+V_{REF} \left( \frac{2047}{2048} \right)$
1000 0000 0001	$+V_{REF} \left( \frac{1}{2048} \right)$
1000 0000 0000	0
0111 1111 1111	$-V_{REF} \left( \frac{1}{2048} \right)$
0000 0000 0001	$-V_{REF} \left( \frac{2047}{2048} \right)$
0000 0000 0000	$-V_{REF}$

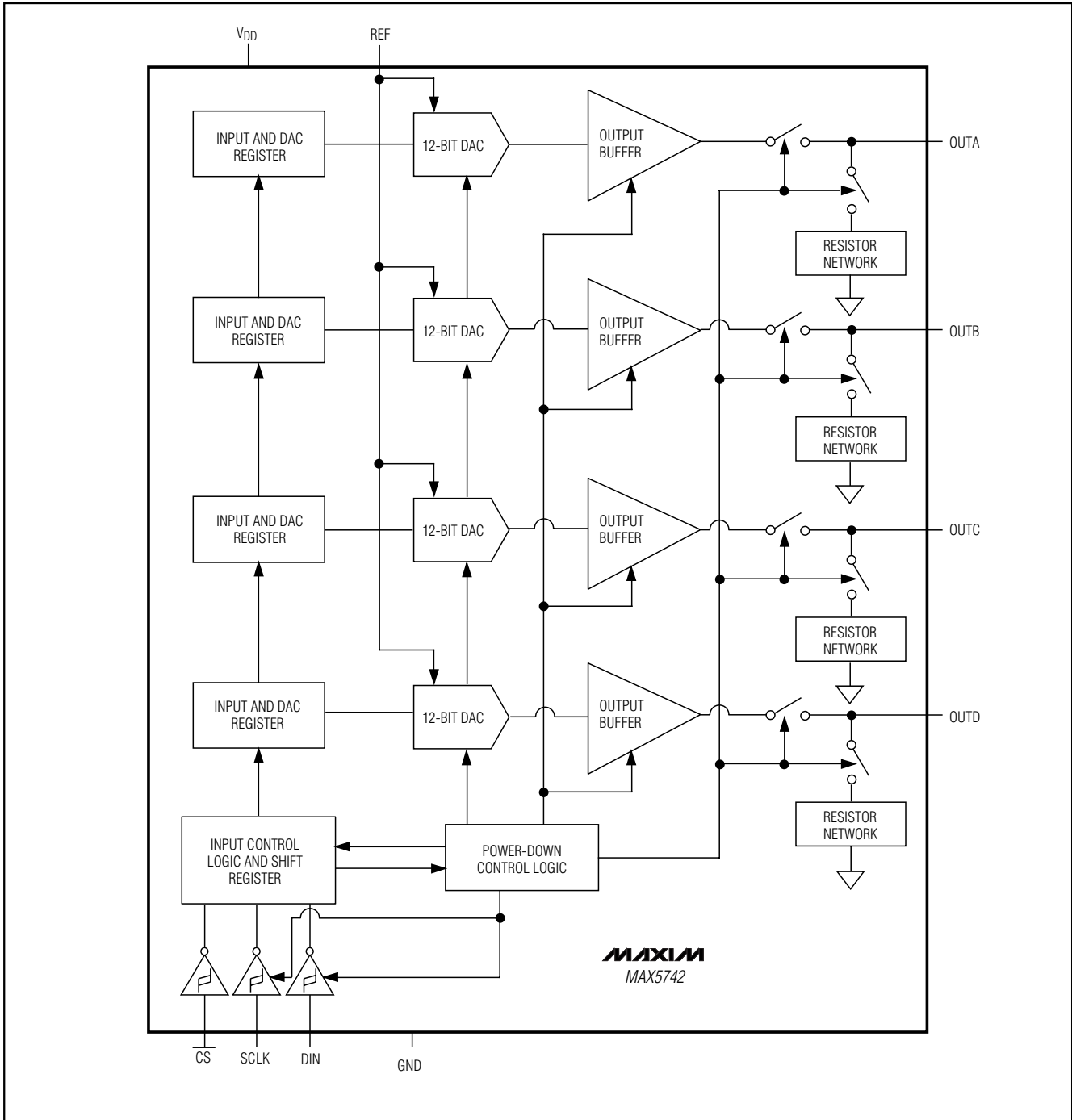
## Chip Information

TRANSISTOR COUNT: 14,458

PROCESS: BiCMOS

# 12-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

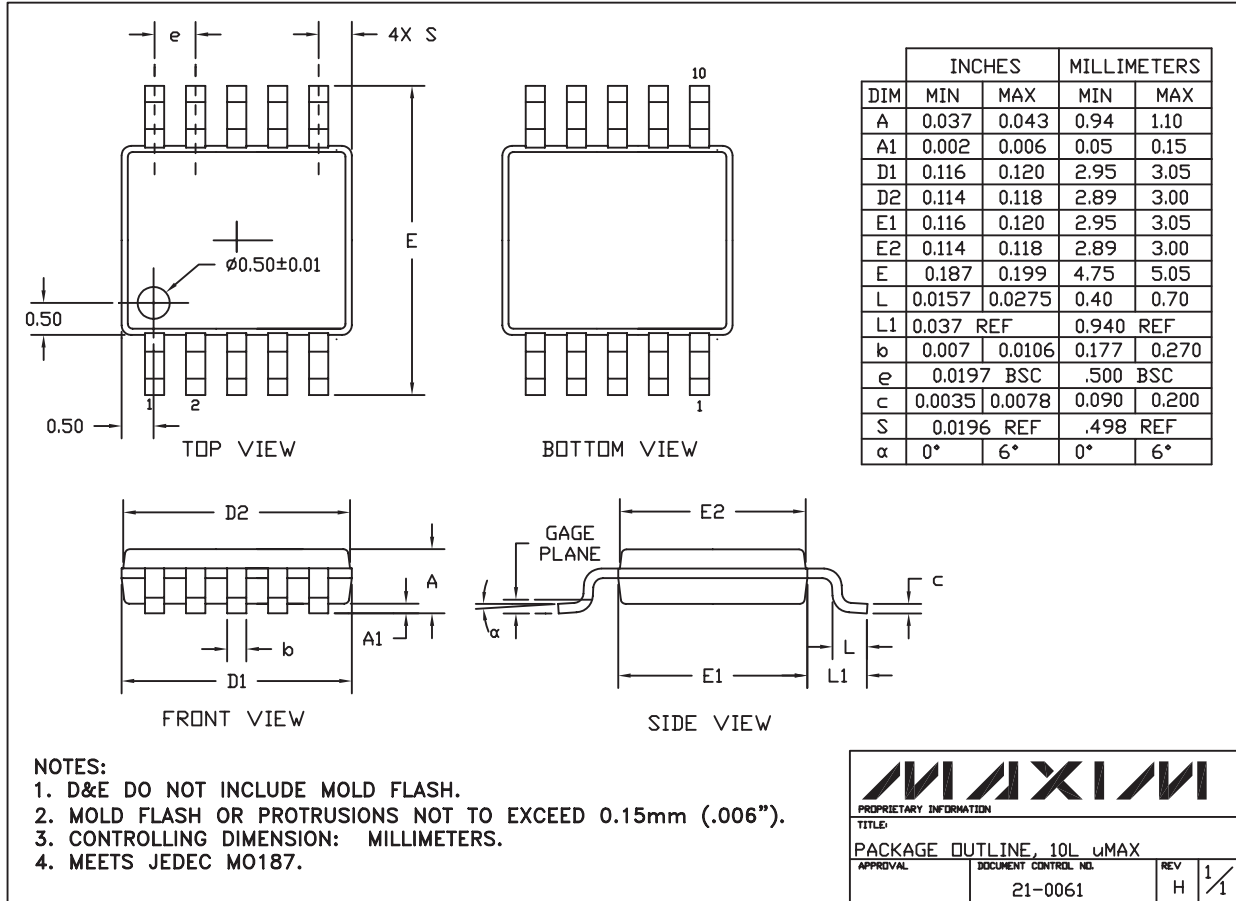
Functional Diagram



# 12-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

## Package Information

**MAX5742**



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